HIP1011 PCI Hot Plug Controller

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Introduction

The HIP1011 was the first device designed to be fully compatible with the PCI Hot Plug specification. This device facilitates “HOT PLUGGING”, the removal or insertion of PCI compliant cards without the need to power down the server voltage bus. The HIP1011 controls all four (-12V, +12V, +3.3V, +5V) supplies found in PCI applications, monitoring and protecting against over current (OC) and under voltage (UV) conditions. Reference the HIP1011 data sheet (4311) and the PCI Hot Plug specification available from www.pcisig.com.

Figure 2 illustrates the typical implementation of the HIP1011. Additional components for optimizing performance in particular applications, ambient electrical noise levels or desired features will be necessary.

The ease of implementation of the HIP1011 Hot Plug Solution (HIP1011 and as few as 2 N-Channel MOSFETs like the ITF86130 UltraFET) is complemented by the small PCB foot print necessary, since both are available in 0.150 inch SOICs. The typical application requires only 1.1 sq. inches of PCB board space (see Figure 1).

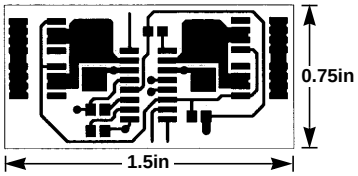

FIGURE 1. LAYOUT PLOT, ACTUAL SIZE (0.75in x 1.5in)

Key Feature Description and Operation

The HIP1011, two power MOSFETs and a few passive components as configured in Figure 2, create a small and simple yet complete power control solution. It provides the maximum specified current for each supply to the PCI adapter slot. Over current monitoring and protection for the 3.3V and 5V supplies is provided by sensing the voltage across external current-sense resistors. For the +12V and -12V inputs, over current protection is provided internally. On-chip references are used to monitor the +5V, +3.3V and +12V outputs for under voltage conditions. During an over current condition on any output, or an under voltage condition on the +5V, +3.3V or +12V outputs, all MOSFETs are immediately latched-off and a LOW (0V) is presented to the FLTN output. During initial power-up of the main V_{CC} supply (+12V), the PWRON input is inhibited from turning on the switches, and the latch is held in the reset state until the V_{CC} input is greater than 10V. If FLTN is latched low and PWRON is cycled low then high, the FLTN latch will clear. User programing of the over current threshold by a resistor connected to the OCSET pin and turn-on slew rate by capacitors connected to the gate pins is provided.

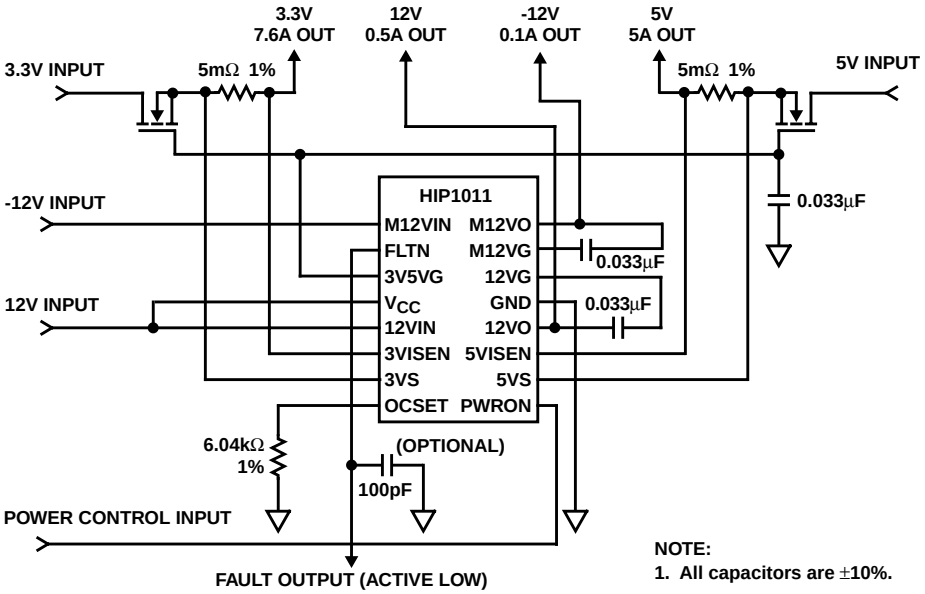

FIGURE 2. HIP1011 TYPICAL APPLICATION

Customizing and Optimizing Circuit Performance

How is the HIP1011 turned on and off?

In a PCI Hot Plug environment the voltages on each individual system slot are controlled by a microprocessor and Hot Plug operating software thus controlling the HIP1011. Reference PCI Hot Plug spec for details. The HIP1011 is designed to turn on, when PWRON (pin 9) voltage >2.1V up to 7.0V and to turn off when <0.8V, making this device controllable using 3V or 5V logic on the dedicated control signal, PWRON.

I keep getting random false fault indications even at low current levels, what should I do? How do I improve noise immunity?

To prevent spurious faults in a noisy electrical environment connect a ≤200pF capacitor between FLTN pin and GND to provide the necessary filtering.

I need to monitor and report the presence of the -12V supply. How do I do that?

With the addition of a small number of external components the monitoring and reporting of the -12V status is possible. In Figure 3 as an example, the M12PG node voltage will be +5V when the -12V supply is out of specification. The addition of C_{GS} allows for a programmable delay in setting M12PG node high. The choice of component values determines the UV signal level.

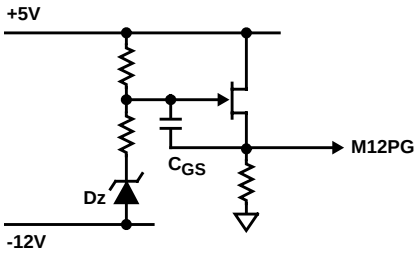

FIGURE 3.

How does the over current set function work, how do I design for different (non PCI) OC limits, and what considerations are there? (See Table 1 for reference.)

The HIP1011 allows easy custom programming of the over current (OC) levels of all 4 supplies by simply changing the resistor value between OCSET, (pin 8), and ground. The R_{OCSET} value and the OCSET 100µA current source set a voltage that is used in 4 comparators, one for each supply. The voltages developed across the 3.3V and 5V sense resistors are applied to the inputs of their respective comparators. The +12V and -12V currents are sensed internally with pilot devices. Once any comparator trips, that output is fed through logic circuits resulting in the FLTN, pin 2, going low, indicating a fault condition. Because of the internal current monitoring of the +12V and -12V switches, their programming flexibility is limited to R_{OCSET} changes.

The 3.3V and 5V over current trip points depend on both R_{OCSET} and the value chosen for each sense resistor.

Over current design guidelines and recommendations are as follows:

1. For PCI applications, set R_{OCSET} to 6.04kΩ, and use 5mΩ 1% sense resistors (see Figure 2).
2. For non PCI applications, the following precautions and limitations apply:

A. **Do not** exceed the maximum power of the integrated NMOS and PMOS. High power dissipation must be coupled with effective thermal management. The integrated PMOS has an $r_{DS(ON)}$ of 0.3Ω. Thus, with 1A of load current the power dissipation is 0.3W. The thermal impedance of the package is 100 degrees per watt, limiting the average DC current on the 12V supply to about 1.5A and imposing an upper limit on the R_{OCSET} resistor. **Do not** use an R_{OCSET} resistor greater than 15kΩ.

The average current on the -12V supply is only limited by electromigration. The average current should not exceed 0.7A. Since the thermal restrictions on the +12V supply are more severe, the +12V supply restricts the use of the HIP1011 to applications where the ±12V supplies draw relatively little current. Since both supplies only have one degree of freedom, the value of R_{OCSET}, the flexibility of programming is quite limited. See the HIP1011B data sheet.

B. **Do not** try to sense voltages across the two external sense resistors that are less than 33mV. Spurious faults due to noise and comparator input sensitivity may result. The minimum R_{OCSET} value is 6kΩ. This will set the 3.3V comparator threshold at 45mV and at 35mV for the 5V comparator. This is the voltage level at which the OC fault (I_{OUT} x R_{SENSE}) will occur.

C. Minimize V_{RSENSE} loss so as to not significantly reduce the voltage delivered to the adapter card. Remember PCB trace and connector losses also need to be considered. Make sure that the R_{SENSE} resistor can handle the power. For best results use a precision resistor with a low temperature coefficient.

D. Minimize external FET $r_{DS(ON)}$. Two ITF86130 MOSFETs in parallel are recommended.

EXAMPLES:

Two design examples focusing on different critical requirements are offered below.

Example 1: PCI Applications.

Figure 2 meets all PCI specifications for slew rate and over current protection.

Example 2: Custom over current levels.

1. Choose ROCSET to give acceptable over current trip points for the ±12V supplies. For repeatable results, Rocset must be greater than 6kΩ. For reliability, ROCSET must be less than 15kΩ. These two over current levels

can not be adjusted independently. As an example, suppose we choose ROCSET = 6kΩ. From Table 1, we find that the 12V supply will trip at approximately 750mA, and the -12V supply will trip at approximately 180mA.

2. Choose the 3V and 5V sense resistors to set the over current level for each supply. For example, if the sense resistor in the 5V supply is 25mΩ, then from Table 1, we can calculate that the over current trip point will be ((100µA x 6kΩ)/17)/(.025) = 1.4A. Similarly, if the sense resistor in the 3.3V supply is 10mΩ then its over current trip point will be 4.5A.

TABLE 1.

SUPPLY	HOW TO DETERMINE NOMINAL (±10%)I_{OC} FOR EACH SUPPLY
+3.3V I_{OC}	((100µA x R_{OCSET})/13.3)/R_{SENSE}
+5.0V I_{OC}	((100µA x R_{OCSET})/17)/R_{SENSE}
+12V I_{OC}	(100µA x R_{OCSET})/0.8
-12V I_{OC}	(100µA x R_{OCSET})/3.3

Does the HIP1011 implementation allow for soft start on the voltage supplies and can I adjust it?

Yes, the HIP1011 implementation does allow the user to select the rate of ramp up on the voltage supplies. This start up ramp minimizes in-rush current at start up while the bulk capacitors charge. The ramp is created by placing a capacitor on M12VG to M12VO, 12VG to 12VO and 3V5VG to ground. These capacitors are each charged up by a nominal 25µA current during turn on. A note of caution when choosing capacitor values. The 3.3V and 5V UV circuitry is enabled after the voltage on 12VG is less than 400mV. Therefore, if the capacitor on the pin 3 (3V5VG) is more than 50% larger than the capacitor on pin 14 (12VG) a false UV may be detected during start up. The same value for all 3 gate timing capacitors is recommended. The minimum value for PCI applications is 0.033µF as a smaller value may cause overcurrent faults at power up.

The gate capacitors must be discharged when a fault is detected to turn off the power FETs. Thus, larger caps slow the response time. If the gate capacitors are too large the HIP1011 may not be able to protect the bus or the power FETs. Doubling the gate capacitance will double the response time. For example, with 0.033µF gate capacitance, the response time will be less than 6µs.

There is both a V_{CC} and a 12VIN pin; what do I do with them, tie them together or leave them separate?

The inclusion of separate pins for V_{CC} and 12VIN is to offer the flexibility in design of the HIP1011 controller function to be either powered by a separate unswitched supply (tie V_{CC} to unswitched supply) or to use the same 12V supply as that being controlled by the HIP1011 (tie V_{CC} to 12VIN).

Ideally, V_{CC} should be filtered by an RC network from 12VIN if both pins are tied to the same supply. This will preclude the possibility a short resetting the power on reset latch.

I have 2 non-PCI Hot Plug applications where I want to control the 3 positive voltage supplies or just the 3.3V and 5V supplies, can I use the HIP1011 for these applications?

Yes, the HIP1011 can be used in these applications. Since the HIP1011 does not self monitor the -12V supply for a UV condition, short the M12VO and M12VG pins together. You now have a +3.3V, +5V and +12V controller with full OC and UV fault monitoring and reporting. By additionally shorting the 12VG pin to the V_{CC} pin to disable the UV feature, the +3.3V and +5V supplies are still monitored for OC events.

Additionally, for +3.3V and +5V control, Intersil also has the HIP1012 hot swap power controller that can control +3.3V and +5V or +5V and +12V.

Can I plug a HIP1011 equipped adapter card into a CompactPCI backplane?

Yes, the HIP1011 can be used on a CompactPCI adapter card application. In the present pin field in the CPCI connector V_{CC}, +12V, -12V, +5V, +3.3V all connect simultaneously after the ground connection is made. A pull down resistor from the PWRON pin to ground ensures that upon positive contact the HIP1011 is initially off and in a stable condition. The last pin to connect is the board present pin which is tied to ground on the backplane. With a 5V logic inverter connected from the board present pin to the HIP1011 PWRON pin, once the board is fully inserted the PWRON state goes high turning on the HIP1011 and powering up the adapter card. See Tech Brief TB358 and the HIP1011EVAL2 board for additional implementation information.

This connection sequence is necessary primarily to prevent the integrated +12V PMOS device from being in an ON state at the time of insertion contact. Due to capacitive load charging, it is likely that excessive dissipated power in the PMOS would occur with possible destruction upon an interrupted insertion cycle. With the described requirement met, the HIP1011 upon positive contact, will be in a stable state with all the bus switches off and awaiting a PWRON signal.

Does the HIP1011 monitor for overvoltage (OV) occurrences on the voltage supply bus?

No, the HIP1011 is designed to work with well behaved bus voltages regulated elsewhere in the system. If OV protection is desired, add a zener diode in parallel with the load. Size the zener to draw current only during the overvoltage. The zener current will latch the HIP1011 off in response to an over voltage condition.

Are there PCB layout design best practices to follow? What are they?

As with most innovative ICs performing critical tasks there are crucial PCB layout best practices to follow for optimal performance. For example (reference Figure 1), the PCB traces that connect each R_{SENSE} must not carry any load current. This can be accomplished by running two dedicated traces directly from the sense resistor to the HIP1011.

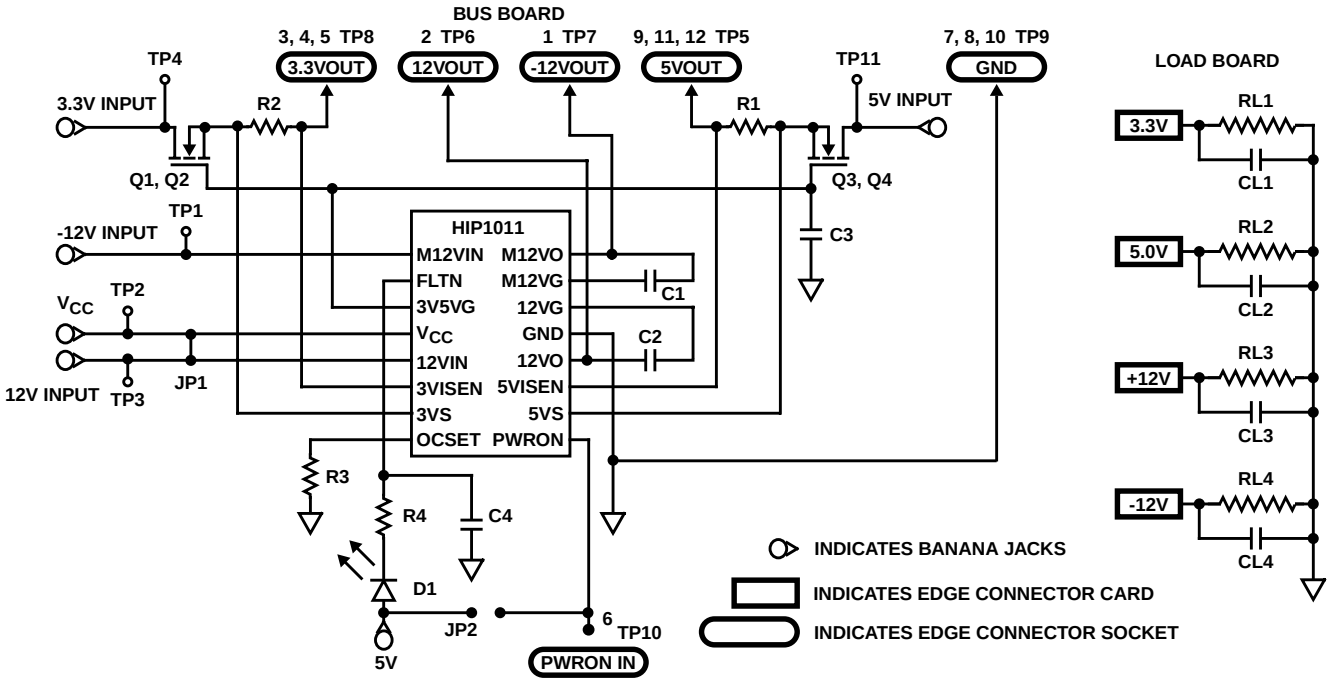

FIGURE 4. HIP1011EVAL1

Is there an evaluation board available?

Yes, there is an evaluation board available through your local Intersil sales office. The HIP1011EVAL1 board (Figure 4) is a simple board designed to demonstrate and evaluate the HIP1011 using an external PWRON signal simulating a PCI Hot Plug environment. The HIP1011EVAL1 board comes in 2 parts, the mother board with the HIP1011, MOSFETs and external components and a load board simulating a 'typical' PCI load with adequate space for modifying the existing load or to add an electronic load. Even with a number of available test points the HIP1011 implementation space is still very efficient. In addition, the demo board offers adequate space to evaluate the application note discussions.

TABLE 2.

COMPONENT DESIGNATOR	COMPONENT NAME	COMPONENT DESCRIPTION
U1	HIP1011CB PCI Hot Plug Controller	Intersil Corporation, HIP1011CB PCI Hot Plug Controller
Q1, Q2, Q3, Q4	RF1K49211	Intersil Corporation, RF1K49211 7A, 12V, 20mΩ, Logic Level N-Channel MOSFET
R1, R2	R_{SENSE} for 3.3V and 5V Supplies	Dale, WSL-2512 10mΩ Metal Strip Resistor
C1, C2, C3	Gate Timing Capacitors	0.033µF 805 Chip Capacitor
R3	Over Current Set Resistor	12.1kΩ 805 Chip Resistor
C4	Fault Stability Capacitor	100pF 805 Chip Cap
Conn. 1	Connector for Load Card	Sullins EZM06DRXH
R4	LED Series Resistor	4.7kΩ 805 Chip Resistor
D1	Fault Indicating LED	Red LED
JP1	V_{CC} to Switched or Unswitched 12V Supply	0.01" Spaced Pins for Jumper Block
JP2	PWRON to 5V	0.01" Spaced Pins for Jumper Block
RL1	3.3V Load Board Resistor	1.1Ω, 10W
RL2	5.0V Load Board Resistor	2.5Ω, 10W
RL3	+12V Load Board Resistor	47Ω, 5W
RL4	-12V Load Board Resistor	240Ω, 2W
CL1, CL2	+3.3V and +5.0V Load Board Capacitor	2200µF
CL3, CL4	+12V and -12V Load Board Capacitor	100µF

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